**DAILY ASSESSMENT FORMAT**

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| **Date:** | **4/June/2020** | **Name:** | **Prashantha naik** |
| **Course:** | **DIGITAL DESIGN USING HDL** | **USN:** | **4al17ec074** |
| **Topic:** | 1. **Hardware modelling using Verilog** 2. **FPGA and ASIC Interview questions** | **Semester & Section:** | **6th b** |
| **Github Repository:** | **prashanth\_course** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.**  **Hardware modelling using Verilog:**     1. **Learnt to model combinational and sequential circuits.** 2. **Distinguish between good and bad coding practices** 3. **Learnt about the Verilog hardware description language** 4. **Distinguish between good and bad coding practices.** 5. **Case studies with some complex designs.**   **Logic design**  **● Generate a netlist of gates/flip-flops or standard cells.**  **● A standard cell is a pre-designed circuit module (like gates, flip-flops, multiplexer, etc.) at the layout level.**  **● Various logic optimization techniques are used to obtain a cost effective design.**  **Moore’s Law**  **● Exponential growth**  **● Design complexity increases rapidly**  **● Automated tools are essential**  **● Must follow well defined design flow**  **FPGA and ASIC Interview questions**    **Implement a simple T Flipflop and test the module using a compiler.** |

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| **Date:** | **4/June/2020** | **Name:** | **Prashantha naik** | |
| **Course:** | **Python** | **USN:** | **4al17ec074** | |
| **Topic:** | 1. **Application 8: Build a Web-based Financial Graph** | **Semester&Section:** | **6th b** | |
| **Git hub repository** | **prashanth\_couse** |  |  | |
| **AFTERNOON SESSION DETAILS** | | | |
| **Image of session** | | | |
| **Report – Report can be typed or hand written for up to two pages.**  **Build a Web-based Financial Graph** | | | |